



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,809	12/31/2001	Ge Nong	01-HK-048 (STMI01-01048)	5323
7590 Lisa K. Jorgenson STMicroelectronics, Inc. 1310 Electronics Drive Carrollton, TX 75006				
EXAMINER				
MURPHY, RHONDA L				
ART UNIT		PAPER NUMBER		
2416				
MAIL DATE		DELIVERY MODE		
12/17/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/036,809

Applicant(s)

NONG, GE

Examiner

RHONDA MURPHY

Art Unit

2416

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 December 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 December 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/08/08 has been entered. Accordingly, claims 1-20 are currently pending.

Response to Arguments

2. Applicant's arguments filed 11/03/08 have been fully considered but they are not persuasive. Applicant argues Krishna fails to teach or suggest a scheduling controller connected to the bufferless, non-blocking interconnecting network, wherein the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network. However, Examiner respectfully disagrees. Krishna teaches a scheduling controller (arbiter 90) connected to the bufferless, non-blocking interconnecting network as illustrated in Figure 1; column 1, lines 22-30 and further described in column 5, lines 8-13. Examiner would like to direct the applicant's attention to figure 1, crossbar 89 and col. 3, lines 63-65 and also col. 6, lines 60-61, in which channels 80-88 form crossbar 89, which does not include any buffers. Thus, producing a bufferless, non-blocking interconnecting network. Furthermore, Krishna teaches the scheduling controller controls the configuration of the bufferless, non-blocking

interconnecting network in column 1, lines 22-30, which recites "*The internal switching fabric of a network device interconnects input ports to output ports and is typically controlled by an arbiter. The arbiter typically controls the flow of data from input to output ports, using an arbitration algorithm to sequentially make matches between the ports. The switching fabric then uses the matches to transfer the data once no more matches can be made. The process of an arbiter controlling a switch fabric to interconnect input and output ports is referred to as "switching" the data.*"

3. Therefore, Examiner's position is that all claim limitations have been met and the rejection has been maintained.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1- 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishna et al. (US 6,563,837).

Regarding claims 1 and 4, Krishna teaches a network device (Fig. 1; device 49) comprising: N input buffers (queues 56, 57, 58) to receive incoming fixed-size data packets from an input port (53) at a first data rate and to output said fixed-size data packets at a second data rate equal to at least twice said first data rate (col. 8, lines 34-

38), wherein said N input buffers are internal to said network device (see Fig. 1) and are external to said input port (see Fig. 1);

N output buffers (queues 65) to receive fixed-size data packets at said second data rate (col. 8, lines 10-15, 34-38) and to output said fixed-sized data packets to an output port (62) at said first data rate (col. 9, lines 6-9), wherein said N output buffers are internal to said switch fabric (see Fig. 1) and are external to said output port (see Fig. 1);

and a bufferless, non-blocking interconnecting network (Fig. 1, col. 3, lines 63-65; col. 6, lines 60-61; channels 80 – 88 form crossbar 89, which does not include any buffers) to receive from said N input buffers said fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N output buffers at said second data rate (col. 8, lines 10-15, 34-38) and

a scheduling controller (arbiter 90) connected to the bufferless, non-blocking interconnecting network (see Fig. 1; col. 1, lines 22-30; further described in col. 5, lines 8-13), wherein the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network (col. 1, lines 22-30).

Krishna fails to explicitly call the network device 49 a switch. However, the network device, which includes the fabric to switch data packets, functions as a switch.

Therefore, it would have been obvious to one skilled in the art to use Krishna's network device as a switch for switching the data packets through the network.

Regarding claims 2 and 5, Krishna teaches a bufferless, non-blocking interconnecting network, comprising a bufferless crossbar (Fig. 1, col. 3, lines 63-65; col. 6, lines 60-61; channels 80 – 88 form crossbar 89, which does not include any buffers).

Regarding claims 3 and 6, Krishna teaches each of said N input buffers is at least twice the size of each of said N output buffers (see Fig. 1).

Regarding claims 7 and 14, Krishna teaches a plurality of fixed-size data packet switches (all elements of Fig. 1, col. 7, lines 35-36), at least one of said fixed-size data packet switches comprising:

N input ports (Fig. 1; ports 53, 54, 55) to receive incoming fixed-size data packets at a first data rate and to output said fixed-size data packets at said first data rate (col. 8, lines 34-38);

N output ports (ports 62, 63, 64) to receive fixed-size data packets at said first data rate (col. 8, lines 10-15) and to output said fixed-sized data packets at said first data rate (col. 9, lines 6-9); and

a network device (device 49; col. 6, lines 60-61) interconnecting said N input ports and said N output ports (see Fig. 1) comprising:

N input buffers (queues 56, 57, 58) to receive incoming fixed-size data packets at a first data rate and to output said fixed-size data packets at a second data rate equal to at least twice said first data rate (col. 8, lines 34-38), wherein said N input buffers are internal to said network device (see Fig. 1) and are external to said N input ports (see Fig. 1);

N output buffers (queues 65) to receive fixed-size data packets at said second data rate (col. 8, lines 10-15, 34-38) and to output said fixed-sized data packets at said first data rate (col. 9, lines 6-9) wherein said N output buffers are internal to said switch fabric (see Fig. 1) and are external to said N output ports (see Fig. 1);

a bufferless, non-blocking interconnecting network (Fig. 1, col. 3, lines 63-65; col. 6, lines 60-61; channels 80 – 88 form crossbar 89, which does not include any buffers) to receive from said N input buffers said fixed-size data packets at said second data rate and to transfer said fixed-size data packets to said N output buffers at said second data rate (col. 8, lines 10-15, 34-38); and

a scheduling controller (arbiter 90) connected to the bufferless, non-blocking interconnecting network (see Fig. 1; col. 1, lines 22-30; further described in col. 5, lines 8-13), wherein the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network (col. 1, lines 22-30).

Krishna fails to explicitly call the network device 49 a switch. However, the network device, which includes the fabric to switch data packets, functions as a switch.

Therefore, it would have been obvious to one skilled in the art to use Krishna's network device as a switch for switching the data packets through the network.

Regarding claims 8 and 15, Krishna teaches a bufferless, non-blocking interconnecting network comprising a bufferless crossbar (Fig. 1, col. 3, lines 63-65; col. 6, lines 60-61; channels 80 – 88 form crossbar 89, which does not include any buffers).

Regarding claims 9 and 16, Krishna teaches each of said N input buffers is at least twice the size of each of said N output buffers (see Fig. 1).

Regarding claims 10 and 17, Krishna teaches a scheduling controller to schedule transfer of said fixed-size data packets from said N input ports to said switch fabric (arbiter 90; col. 8, lines 24-38).

Regarding claims 11 and 18, Krishna teaches a scheduling controller scheduling the transfer of said fixed-size data packets from said N output ports to an external device (col. 8, lines 5-15; 24-38).

Regarding claims 12 and 19, Krishna teaches a scheduling controller scheduling the transfer of said fixed-size data packets from said N input buffers to said bufferless, non-blocking interconnecting network (col. 8, lines 5-15; 24-38).

Regarding claims 13 and 20, Krishna teaches a scheduling controller scheduling the transfer of said fixed-size data packets from said N output buffers to said N output ports (col. 8, lines 5-15; 24-38).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RHONDA MURPHY whose telephone number is (571)272-3185. The examiner can normally be reached on Monday - Friday 9:00 - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on (571) 272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Rhonda Murphy
Examiner
Art Unit 2416

/R. M./
Examiner, Art Unit 2416

/FIRMIN BACKER/
Supervisory Patent Examiner, Art Unit 2416